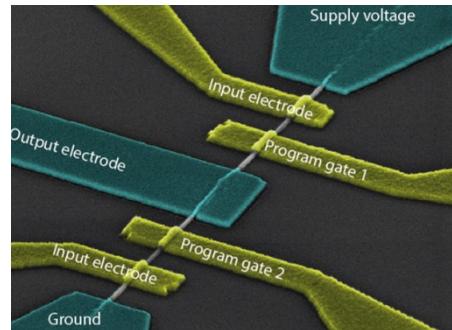


Silicidation and Strain Analysis of Silicon Nanowires

W. M. Weber, M. Löffler,
A. Heinzig, S. Banerjee, W. van Dorp
T. Baldauf, J. Trommer, S. Pregl, U. Mühle
E. Zschech and T. Mikolajick
NaMLab, DCN– TU Dresden,
Fraunhofer IKTS-MD, CfAED

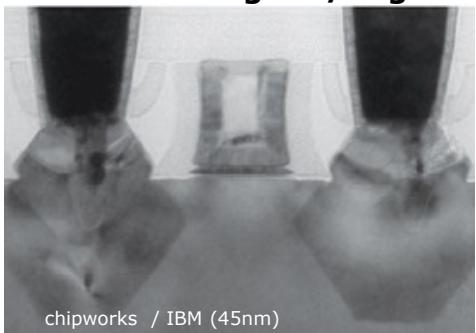


Towards nanowire electronics & nanometer scale silicides

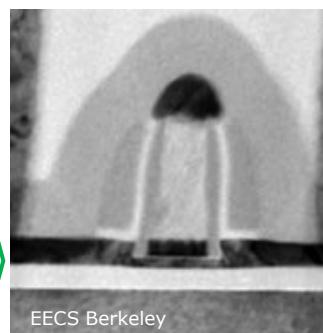
Aim of scaling is to **increase value** each generation

The **scaling path** requires new geometries to reduce short channel effects

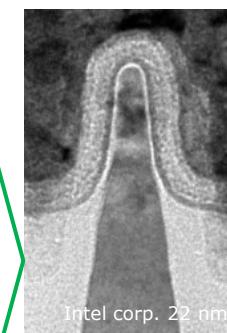
Planar metal gate / high-k



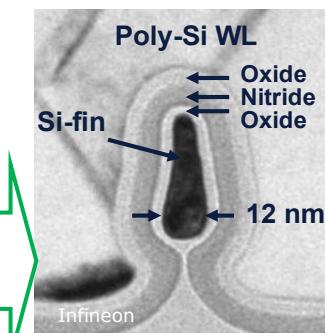
SOI-FET



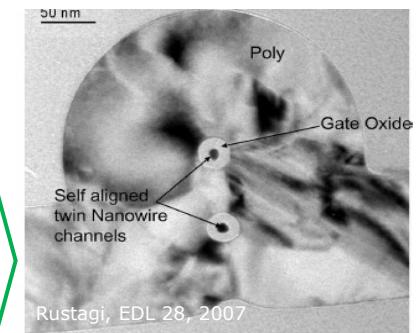
Trigate finFET



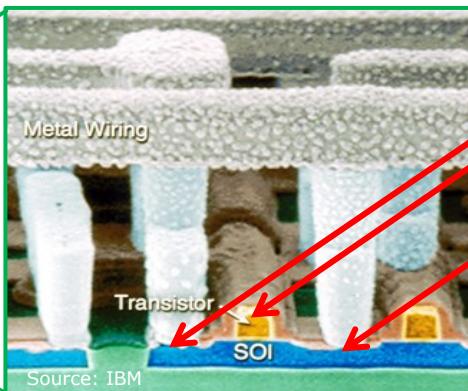
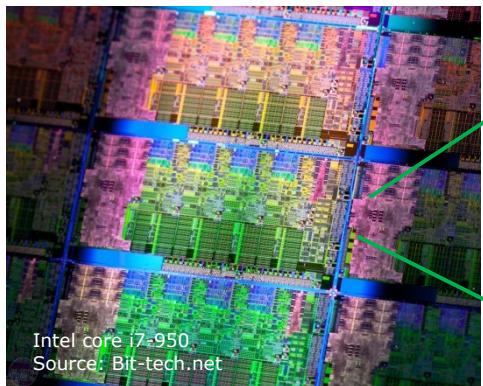
Omega / multi- gate



Nanowire FET



Metal silicides are contact materials to source, drain and gate



Metal silicide

Silicidation and Strain Analysis of Silicon Nanowires

Outline



Metal / silicon nanowire heterostructures



Strained nanowires



Transistor applications



Summary

Silicidation and Strain Analysis of Silicon Nanowires

Outline

Metal / silicon nanowire heterostructures

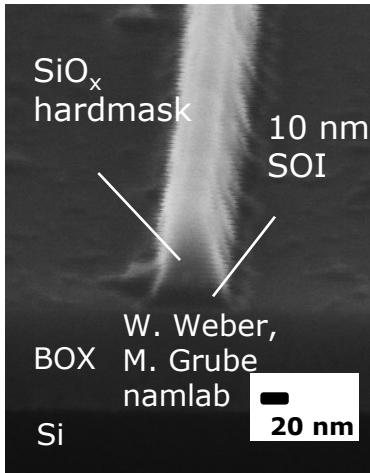
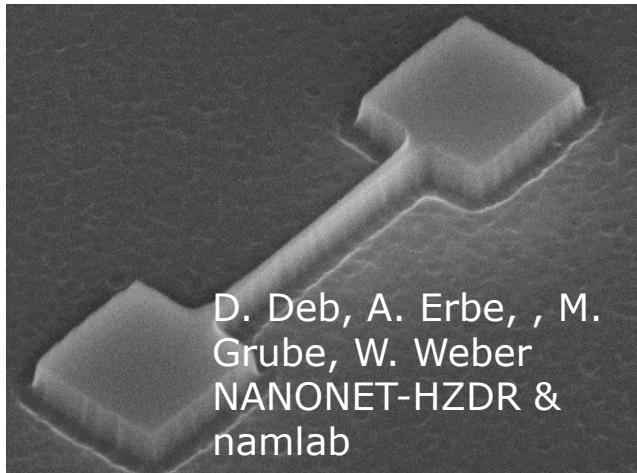
Strained nanowires

Transistor applications

Summary

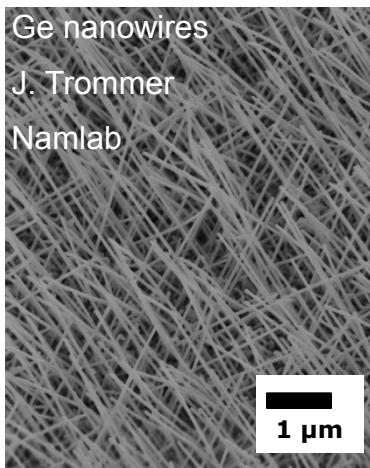
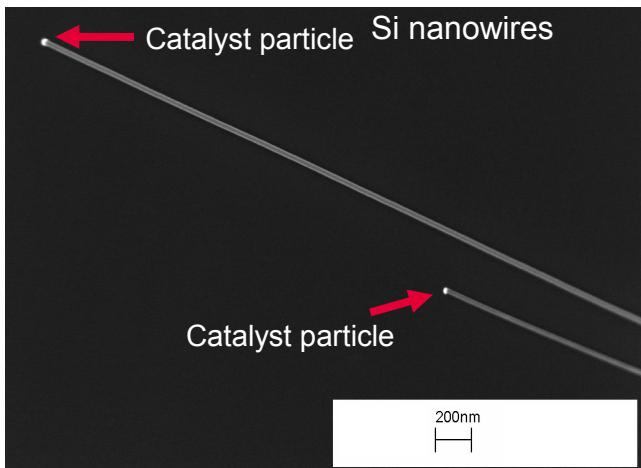
Nanowire and SOI systems employed

Top down



- SOI (10nm d_{Si} on 100nm BOX)
- Defined by lithography & RIE
- Front-end process up to 200 mm wafers
- Prone to surface roughness

Bottom up

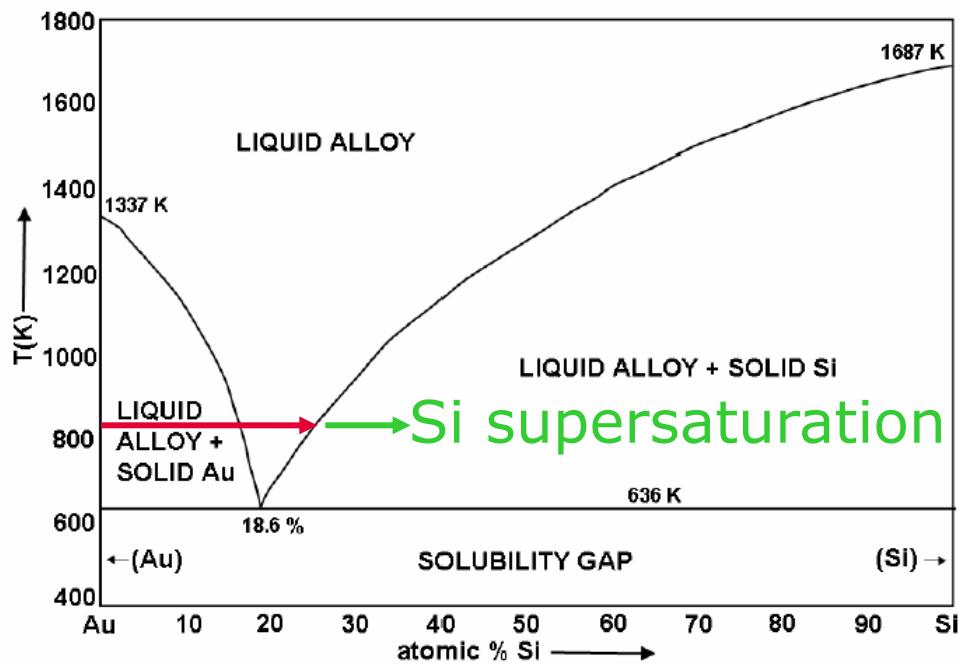


- Diameter down to 5nm defined by seed size
- Controlled crystal orientation:
 $<110>$, $<112>$, $<111>$ Si NW
 $<110>$, $<111>$ Ge NW
- Low surface roughness
- Transfer to test-chip needed
- Simple test vehicle for demonstrators

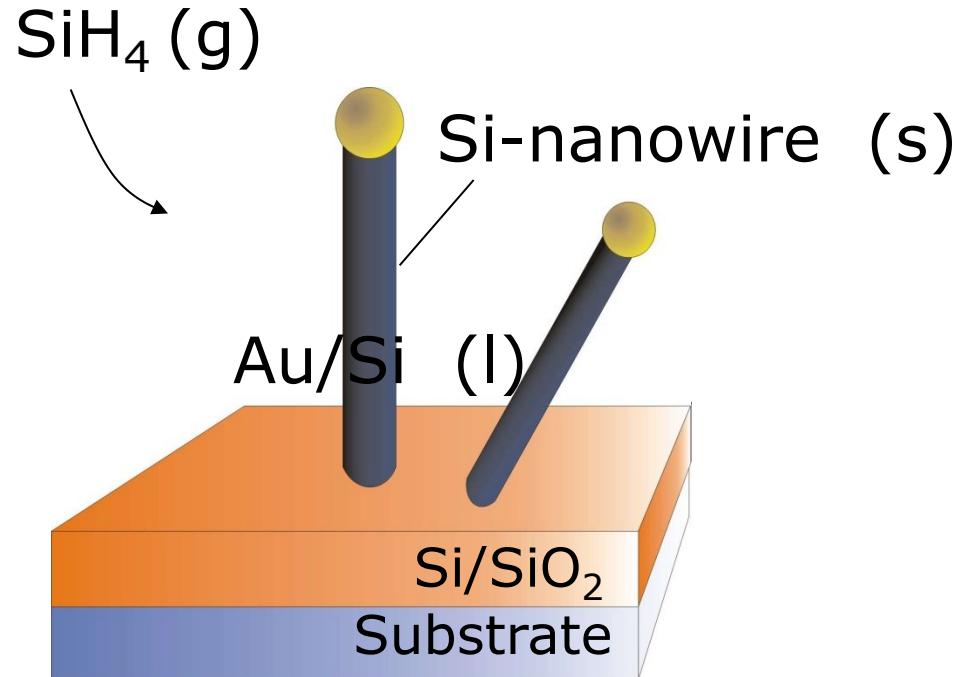
Basic nanowire growth mechanism

Growth: Vapor-Liquid-Solid (VLS) mechanism

Wagner, R.S.; Ellis W.C. Appl. Phys. Lett. 4, 89 (1964)



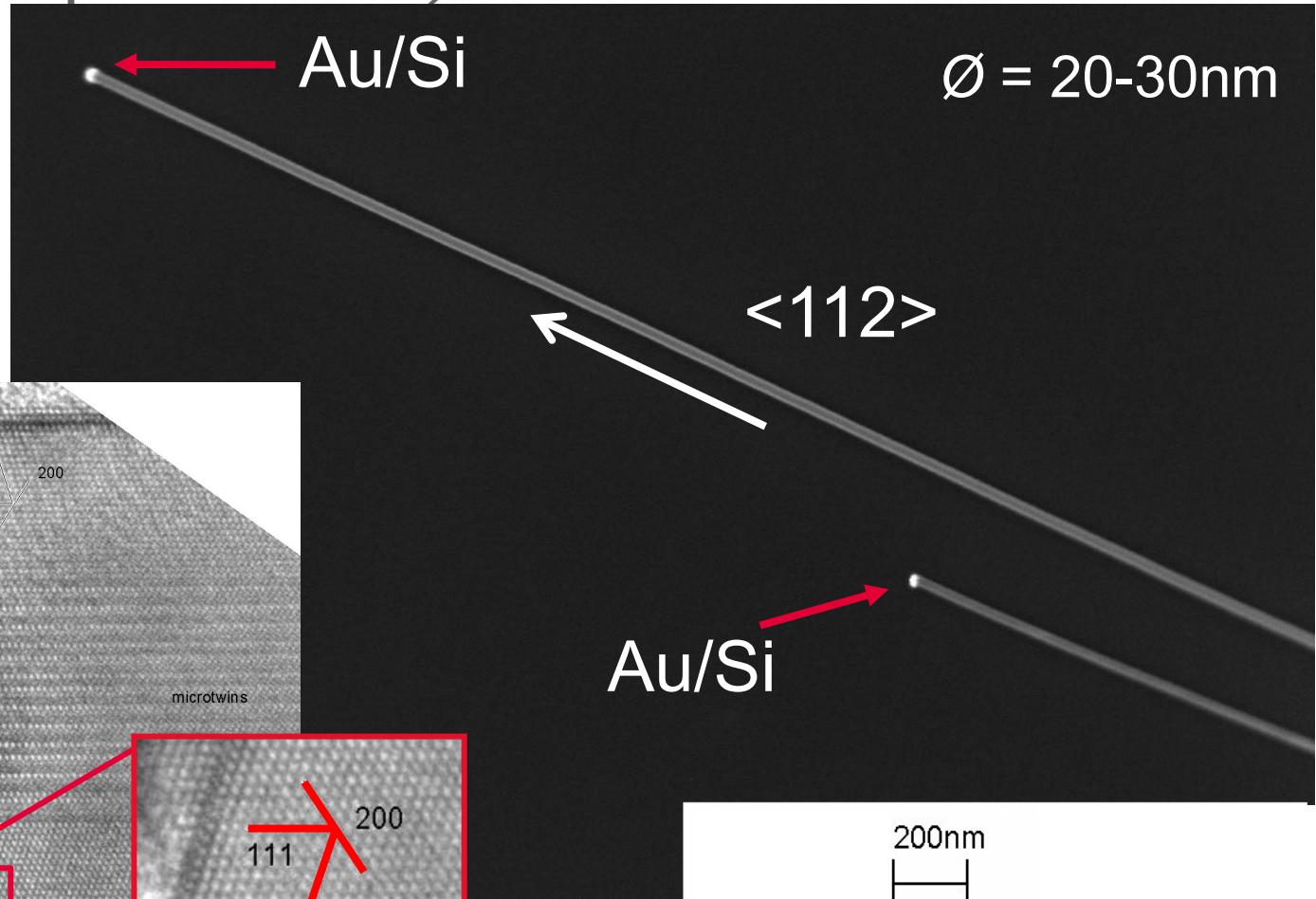
Au/Si eutectic diagram



- Size of clusters define the nanowire's thickness

Intrinsic Si-nanowires (NW) Growth on amorphous SiO₂

- $d_{\text{Au}} = 0.5 \text{ nm}$
- $p_{\text{SiH}_4} = 5 \text{ Torr}$
- $T = 450^\circ\text{C}$
- $\text{g} \sim 7 \mu\text{m} / \text{min}$

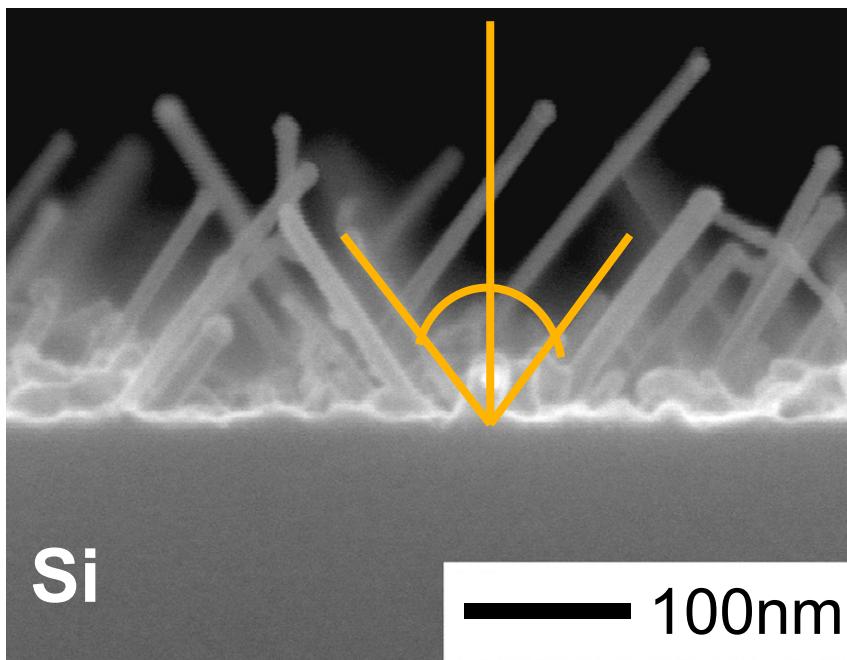


W.M. Weber, et al. IWEPNM 2006
T. Mikolajick, RRL 7, 793 2014

Intrinsic <110> Si-nanowires Growth on crystalline-Si (100)



View in $[0\bar{1}\bar{1}]$

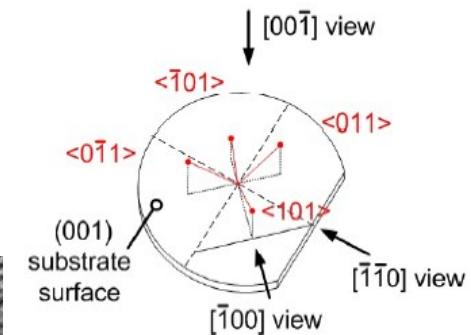
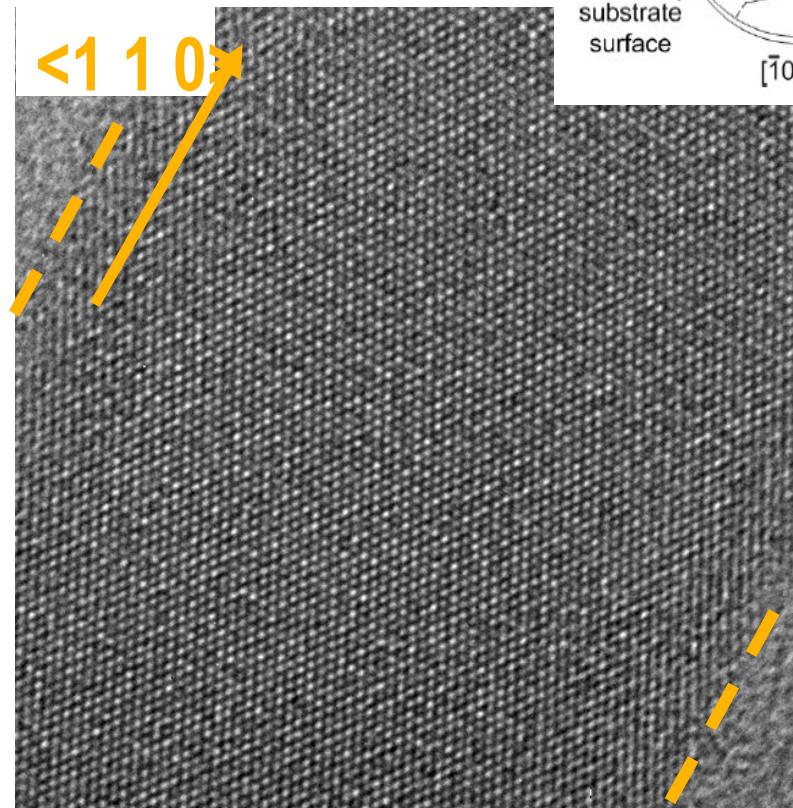


⇒ 0.5 nm Au

⇒ Oriented growth in <110>

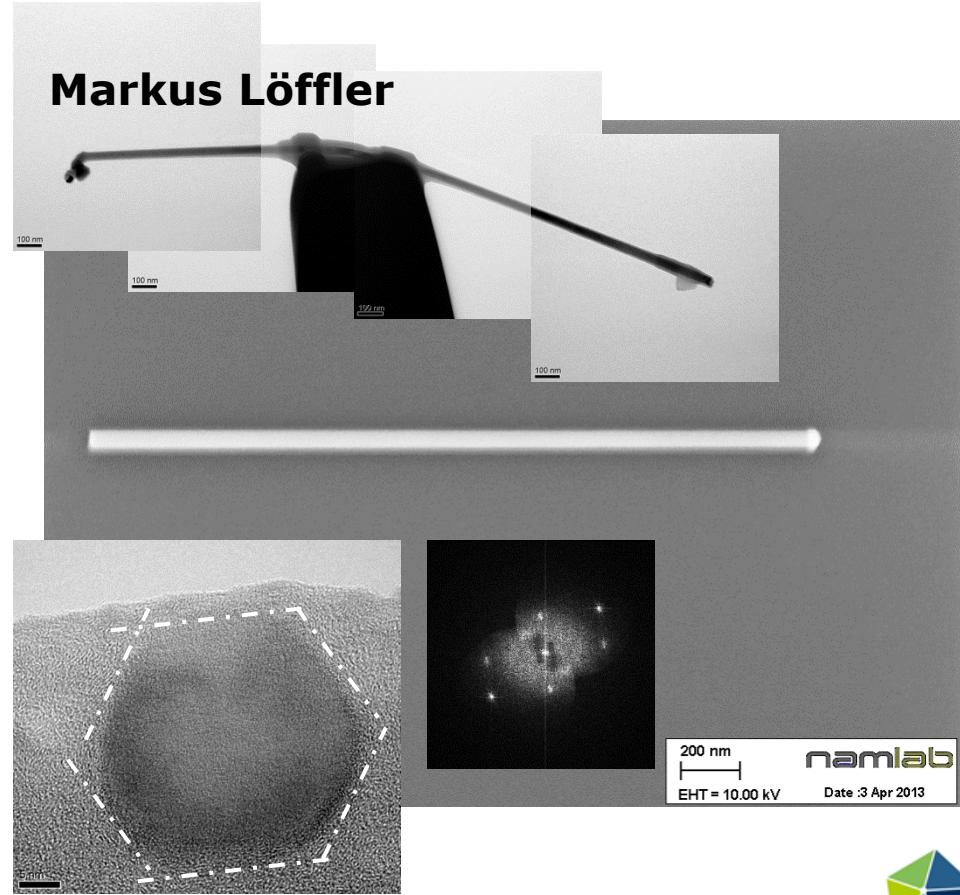
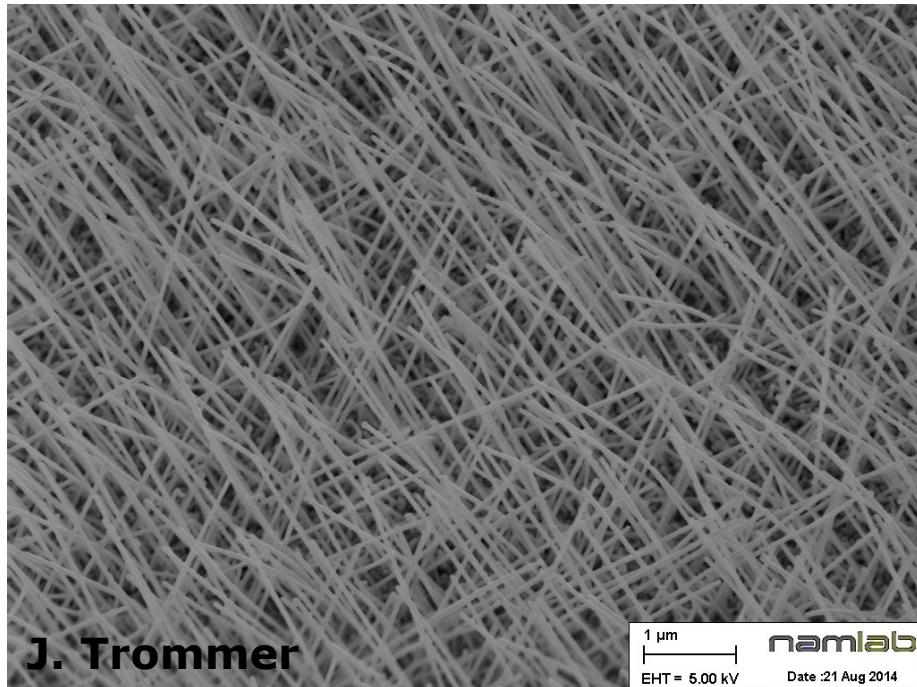
Weber, W. et al. *Phys. Stat. Sol. b.* 243, 3340-3345 (2006).

$\varnothing=25\text{nm}$

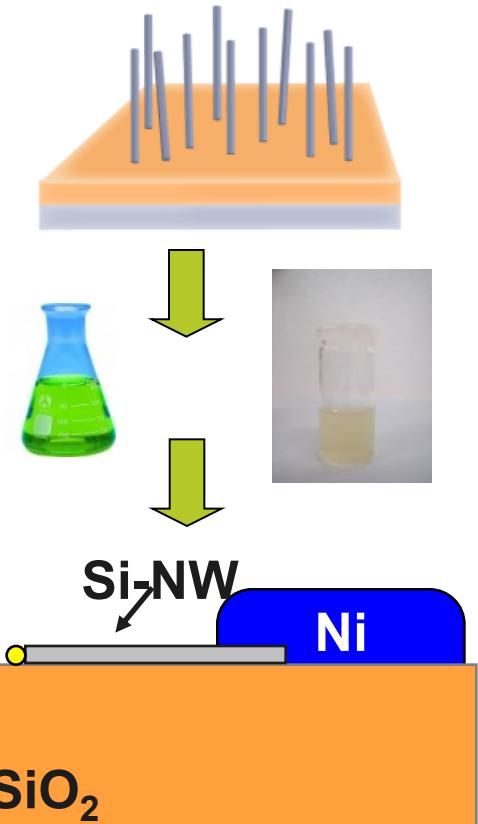
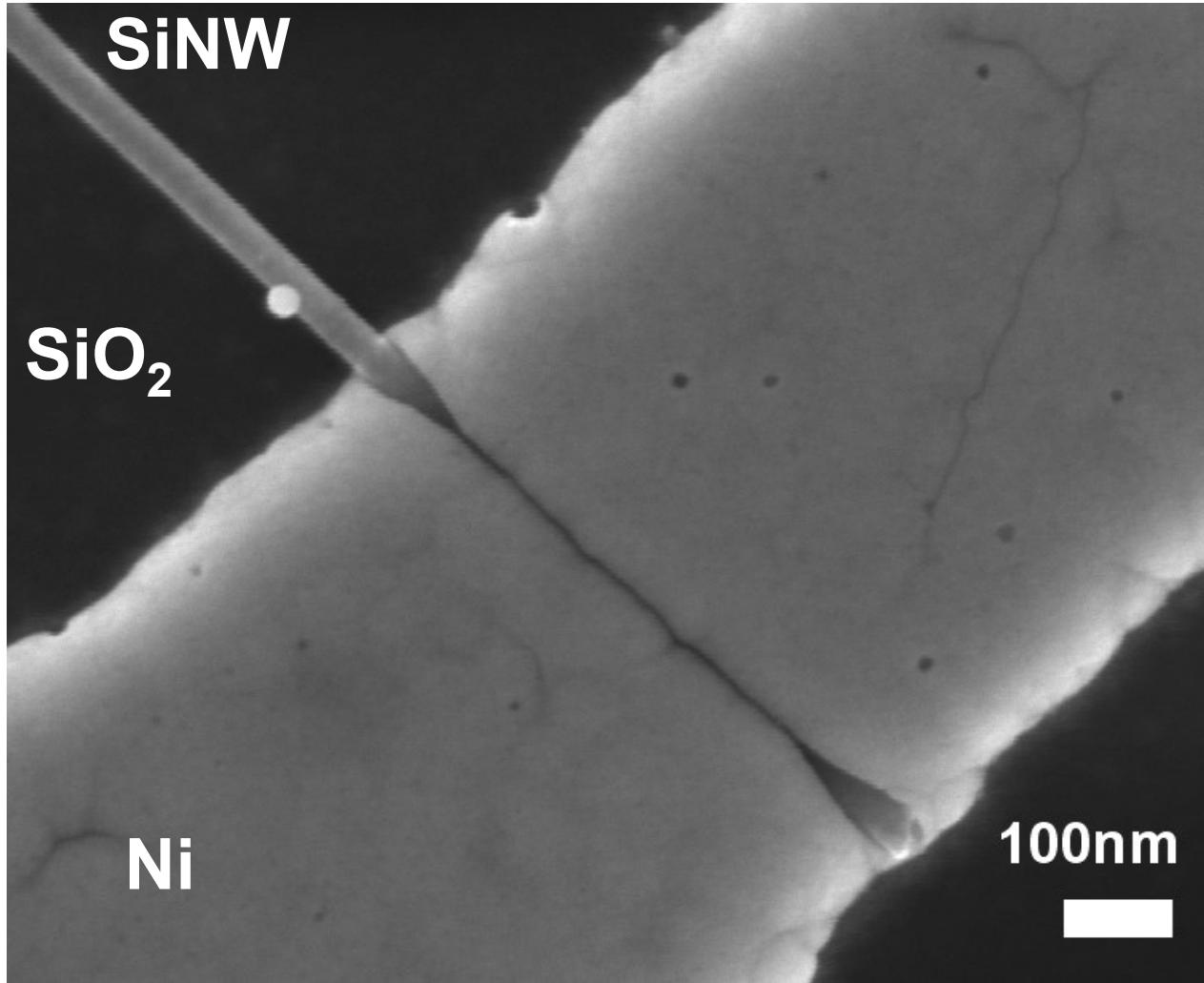


Ge Nanowire growth

- ⇒ Nominally intrinsic Ge NWs on Ge / Si substrates
- ⇒ Pick & place w. manipulator, cross section preparation in ultra-low voltage FIB
- ⇒ $<111>$ axis w. 6-fold sidewall facetting

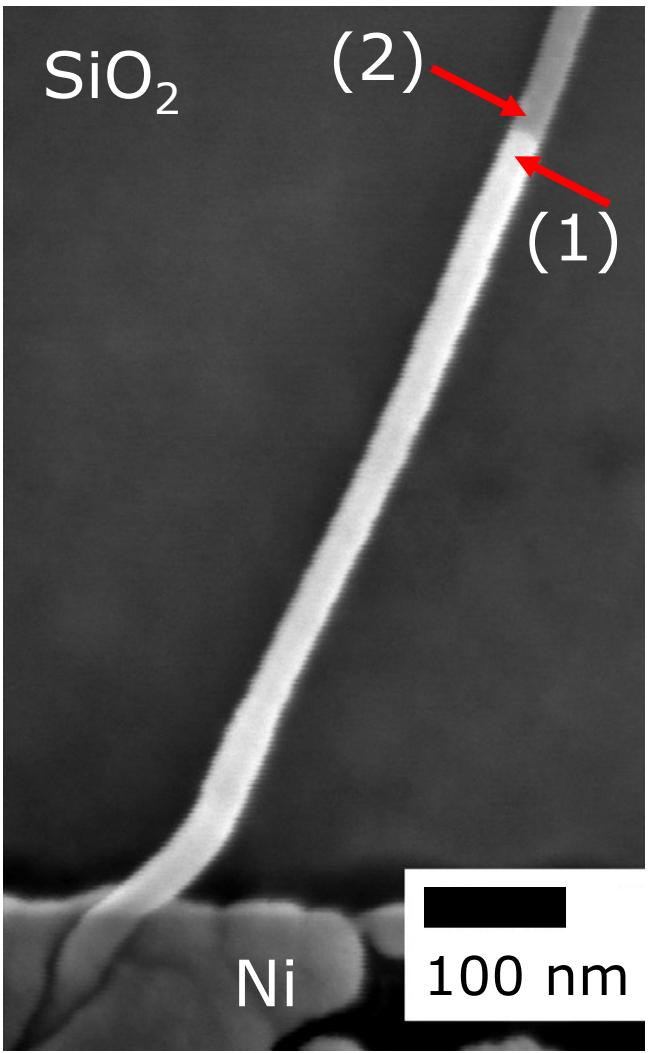


Longitudinal silicidation: Deposition of Ni reservoir



- Contact NWs with Ni reservoirs (plated or deposition)
- Diffusion from an unexhaustible Ni reservoir

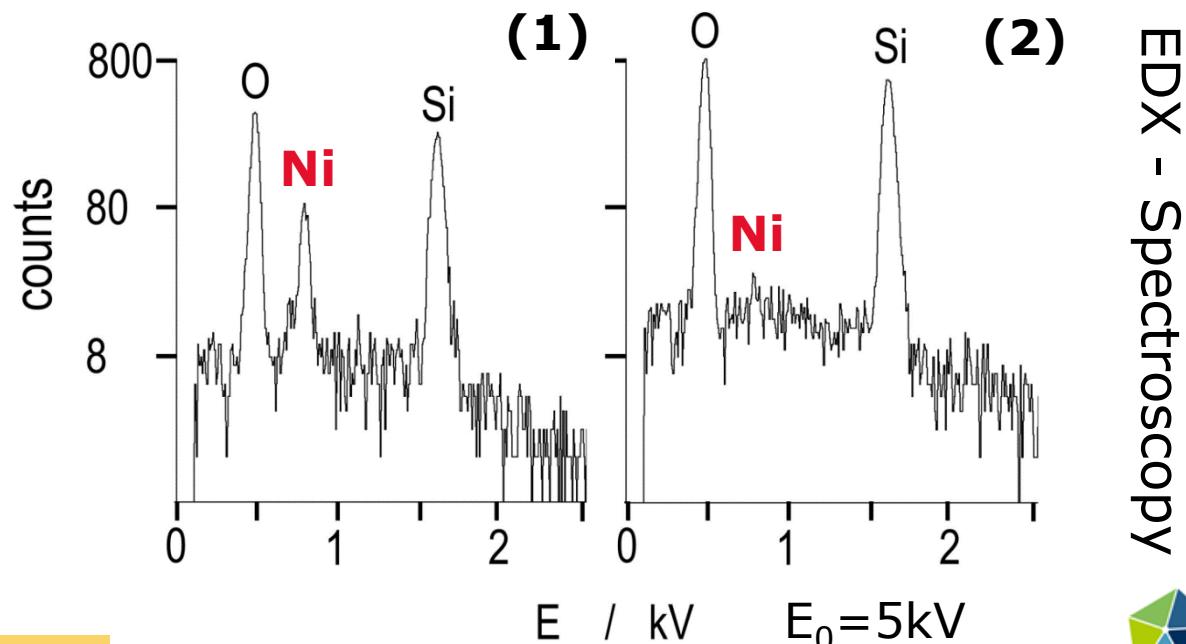
Longitudinal Ni-silicidation over long range



W.M. Weber et al. *Nano Lett.* **6**, 2660 (2006)

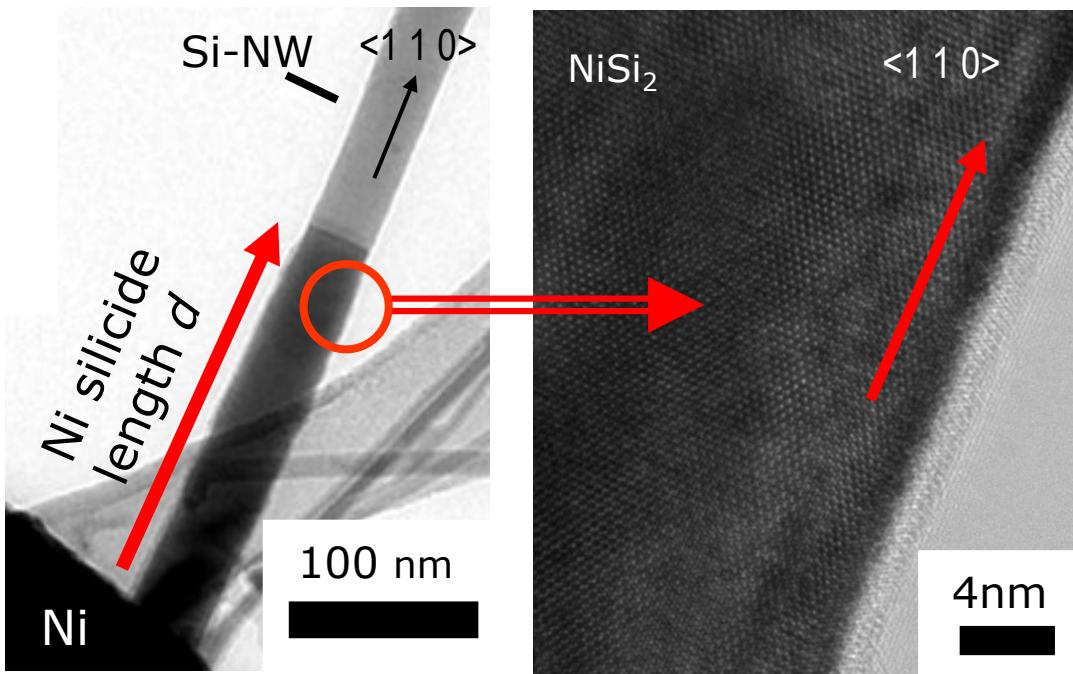
First observation of:

- Longitudinal intrusion of Ni over long distances $\sim 1\mu\text{m}$ Ni-diffusion length
- Formation of sharp interfaces
- Different phase formation in different NWs



Anisotropic Ni silicidation in nanowires

Case 1.- <110> Si nanowires



Process

RTP at 480°C with inexhaustible Ni source.
<110> Si nanowire diameter.

Properties:

- ⇒ Direct NiSi₂ formation without intermediate phases
- ⇒ Single crystal cubic CaF₂ structure of NiSi₂ grown epitaxially on <110> Si
- ⇒ Sharp NiSi₂ / Si interface
- ⇒ - 0.4 % lattice mismatch to Si <111>

Reaction kinetics from in-situ TEM at ~420°C
Volume interstitial diffusion of Ni

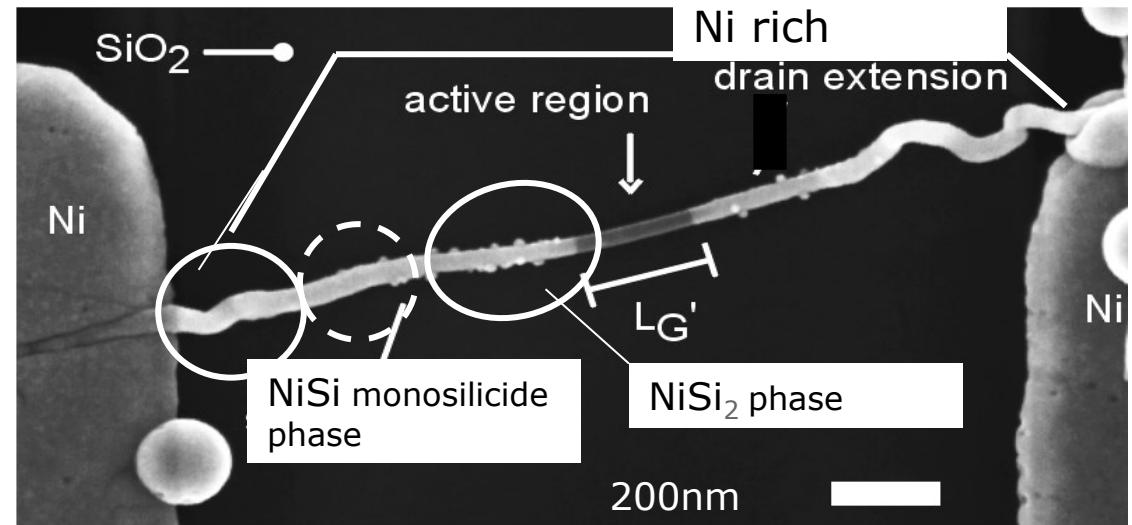
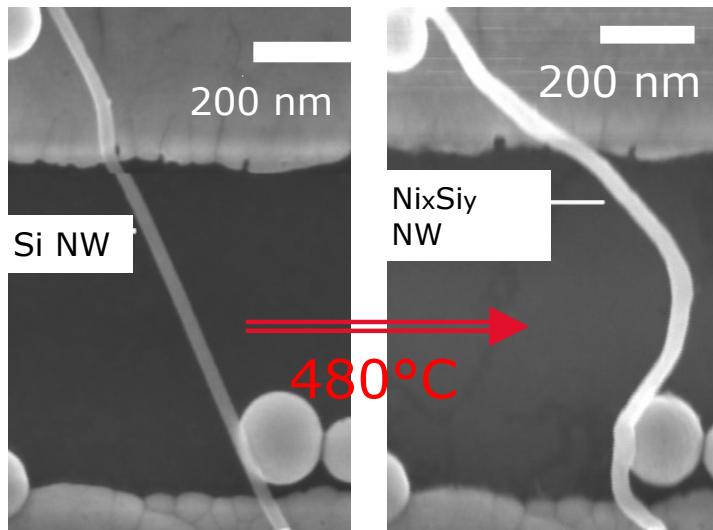
A) Long range $\gg 1\mu\text{m}$ length,
diffusion limited: $d \sim \sqrt{t}$

B) Short range $< 1\mu\text{m}$ length,
reaction limited: $d \sim t$

W.M. Weber et al. *Nano Lett.* **6**, 2660 (2006)

Case 2: Ni silicidation of <112> Si nanowires

<112> nanowire



Elongation of NWs by ~ 30%

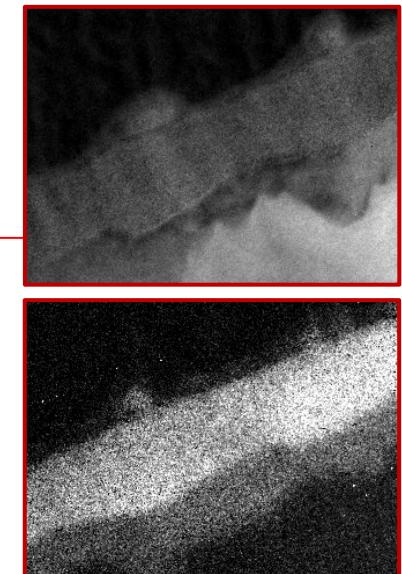
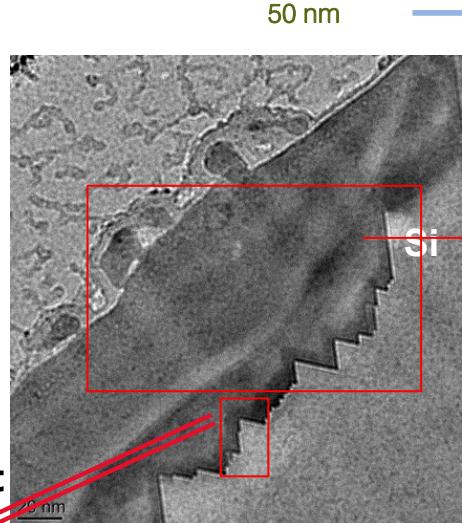
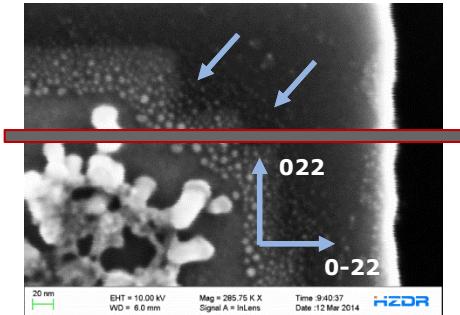
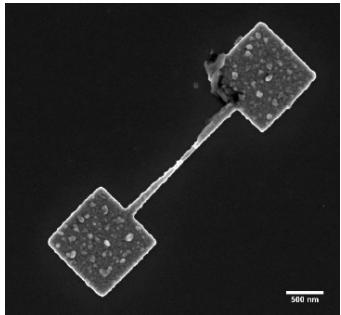
Sequential evolution of 3 different phases

- ⇒ Different segments are formed
- ⇒ Apparently NiSi₂ forms first, followed by two other phases
- ⇒ A sequence of phases form, similar to that of bulk and thin films

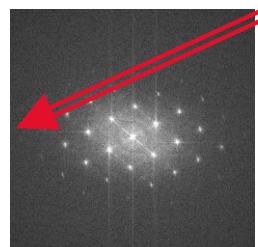
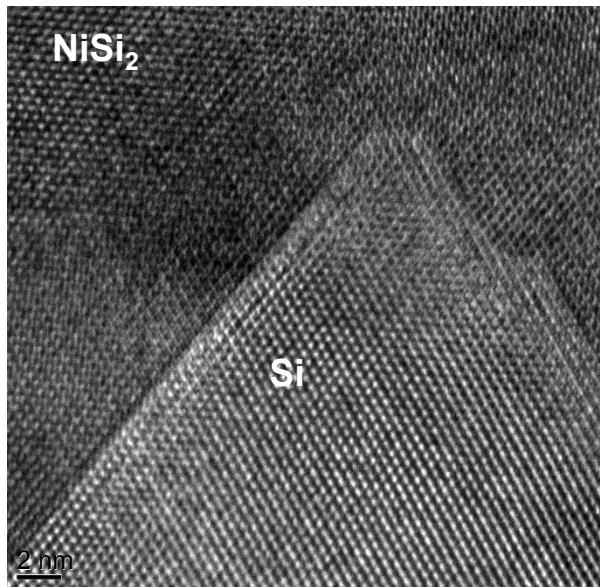
- ⇒ However: In flash anneal no evident formation of different phases

Ni silicidation of bulk Si with inexhaustible Ni source

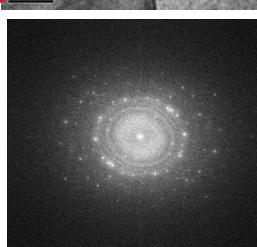
Anneal at 480°C



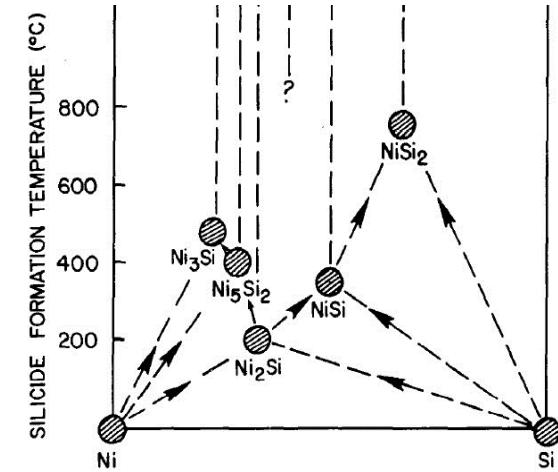
D. Deb, M. Grube, A. Erbe, M. Helm Nanonet



B) NiSi₂ zone axis (1-10)
200
0-22



A) Ni₃₇Si₂₃ complex zone axis (1-10)



Adapted from K.N. Tu
K.N. Tu Ann. Rev. Mater. Sci. 1985, 15: 147

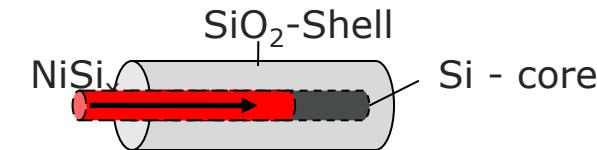
S. Banerjee, E. Zschech, M. Löffler DCN TU-Dresden

Nickel silicide reactions in Si nanowires w. radial compressive strain

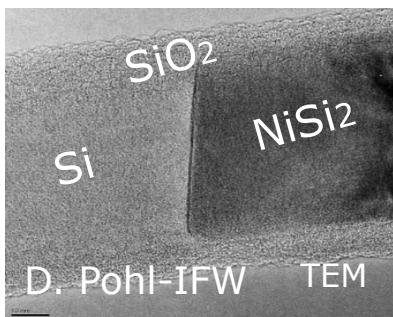
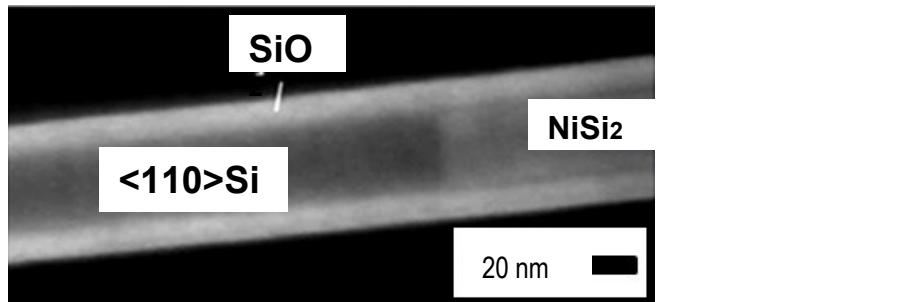
Process:

Thermally grown SiO_2 prior to silicidation (875°C).

Oxidation induces radially compressive strain $\sim 1.3 \text{ GPa}$ into Si core



Case 1.- <110> nanowires



- NiSi_2 formation, no fracturing of shell even for long $> 1\mu\text{m}$ silicide length

Case 2.- <112> nanowires

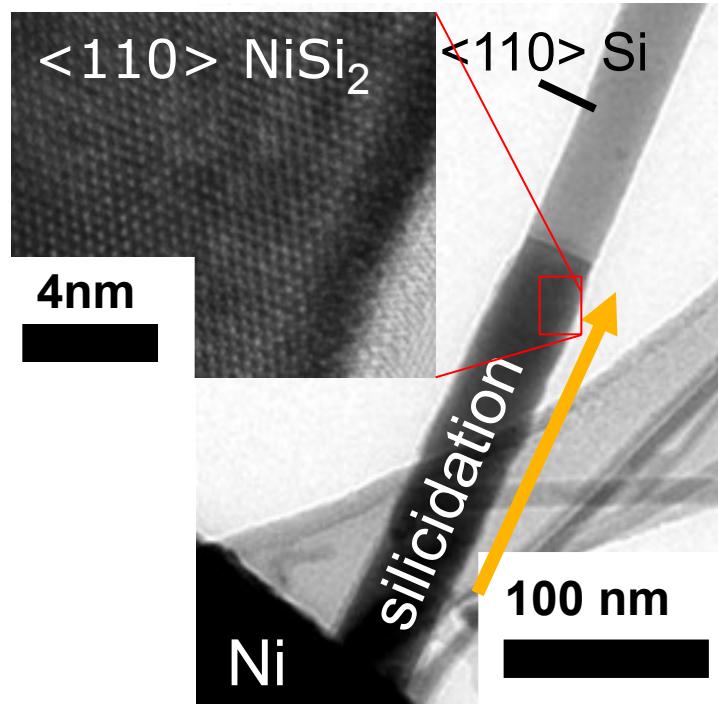


=> Follows similar phase behavior than without shell

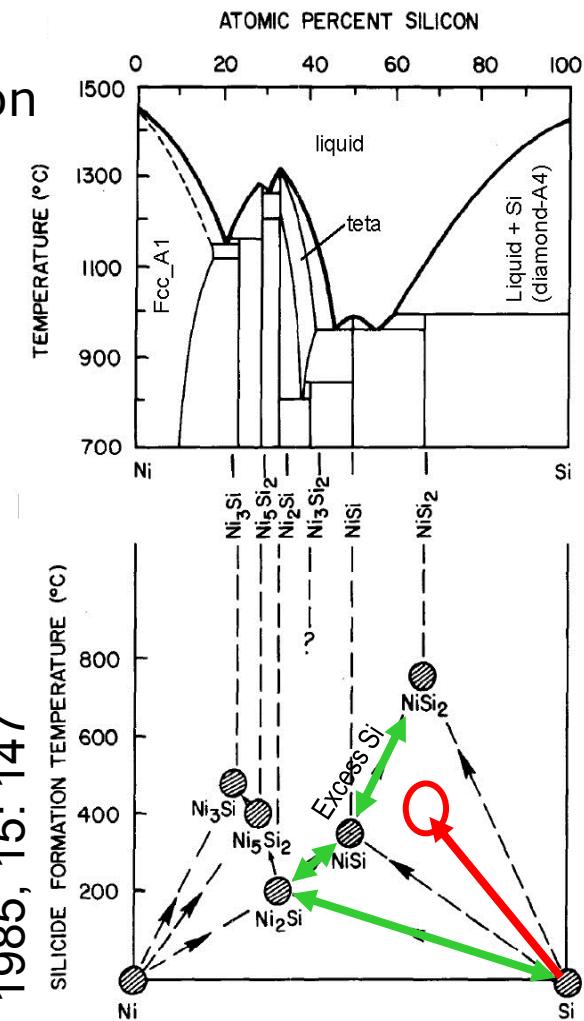
Summary– NixSiy nanowire heterostructures

- Phase formation dependent on crystal orientation:

- <110> -> Direct cubic NiSi_2 lattice matched nucleation
 - 0.4 % lattice mismatch to Si <111>
- <112> -> Sequence: Ni_2Si / NiSi / NiSi_2



W.M. Weber et al. *Nano Lett.* **6**, 2660 (2006)



Adapted from K.N. Tu
K.N. Tu Ann. Rev. Mater. Sci.
1985, 15: 147

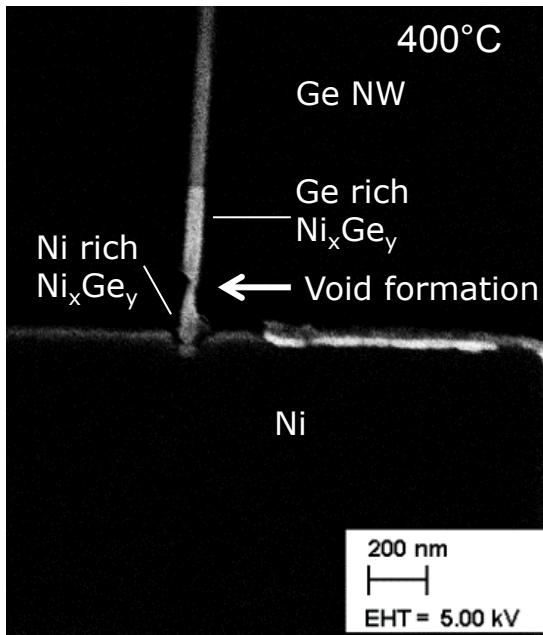
Nickel germanide reactions in Ge nanowires

Process:

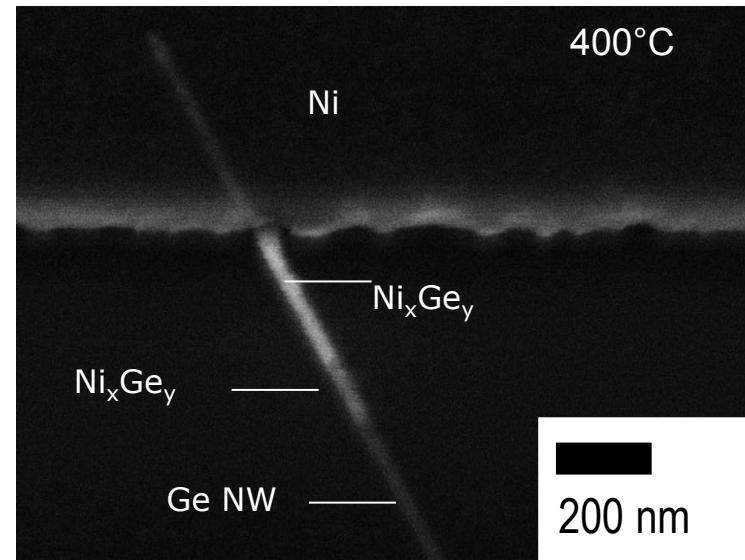
<111> Ge nanowires

RTP at different temperatures 300-400°C

- **Uncapped Ge nanowire**



- **Capped Ge nanowire**

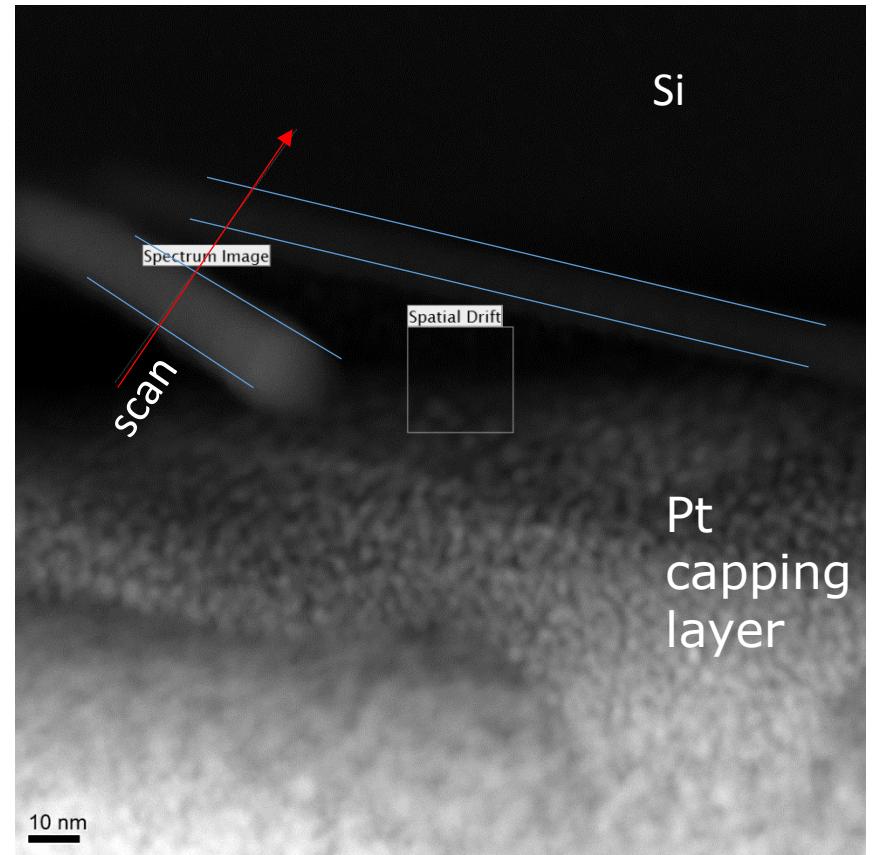
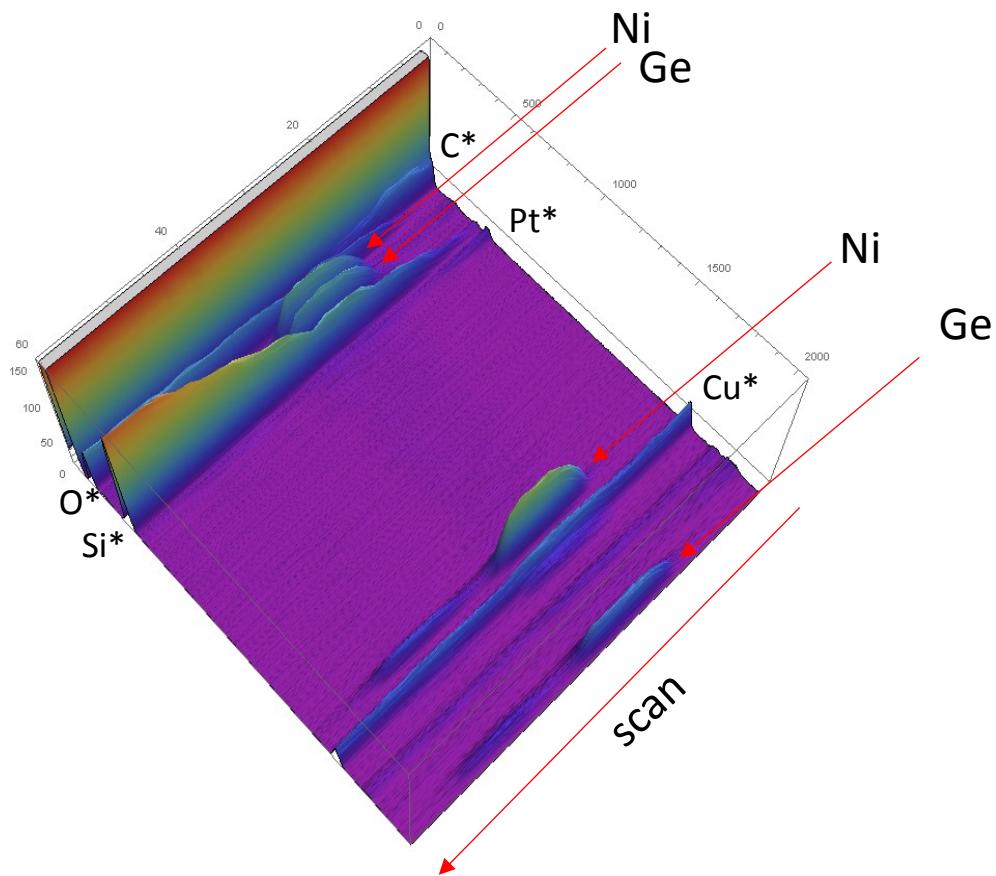


- Strong surface diffusion on Ge nanowires results in void formation

- Capping in ALD Al₂O₃ or Si prevents surface diffusion: no voids formed

Ni_2Ge nanowire segments at the Si junction

TEM EDX profile on longitudinal lift-out lamella



Silicidation and Strain Analysis of Silicon Nanowires

Outline



Metal / silicon nanowire heterostructures



Strained nanowires



Transistor applications



Summary

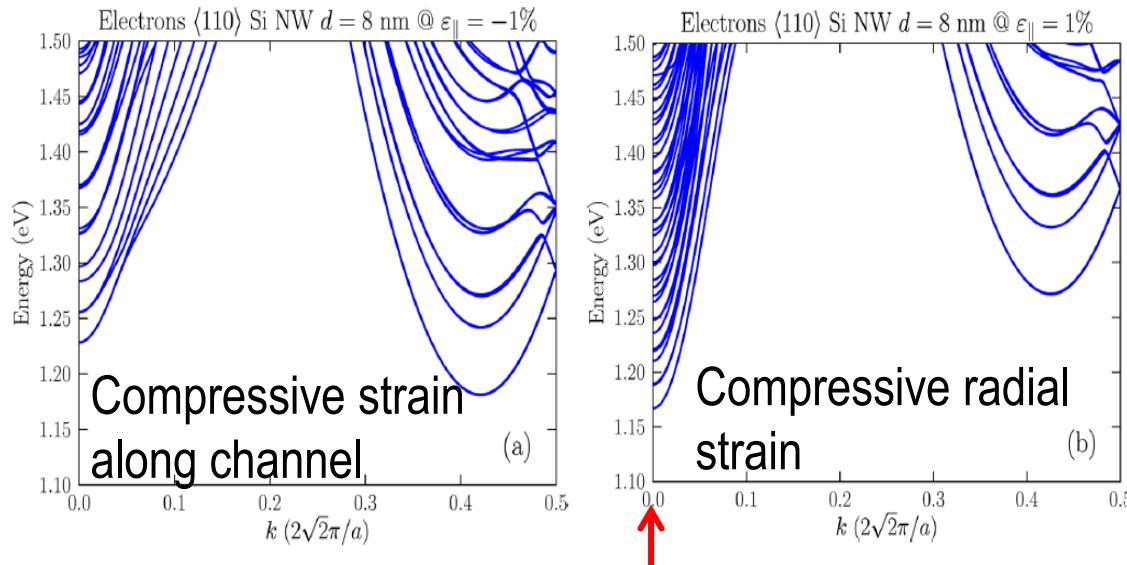
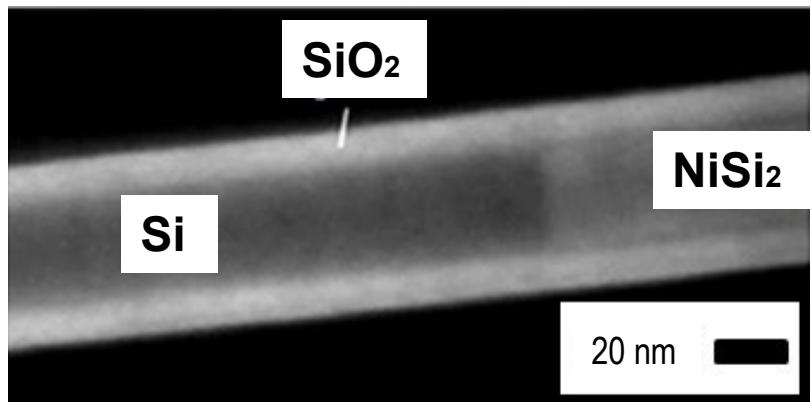
Influence of Strain on Electronic properties of $<110>$ Si NWs

$<110>$ highly sensitive to strain

Radial compressive strain by oxidation

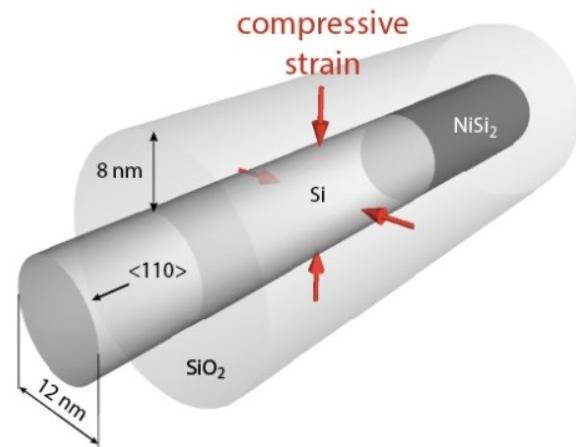
Ec: lowering of light Γ valleys (~ 50 meV)

Split Δ_z m^* drops from 0.19 to $\sim 0.076 m_0^*$



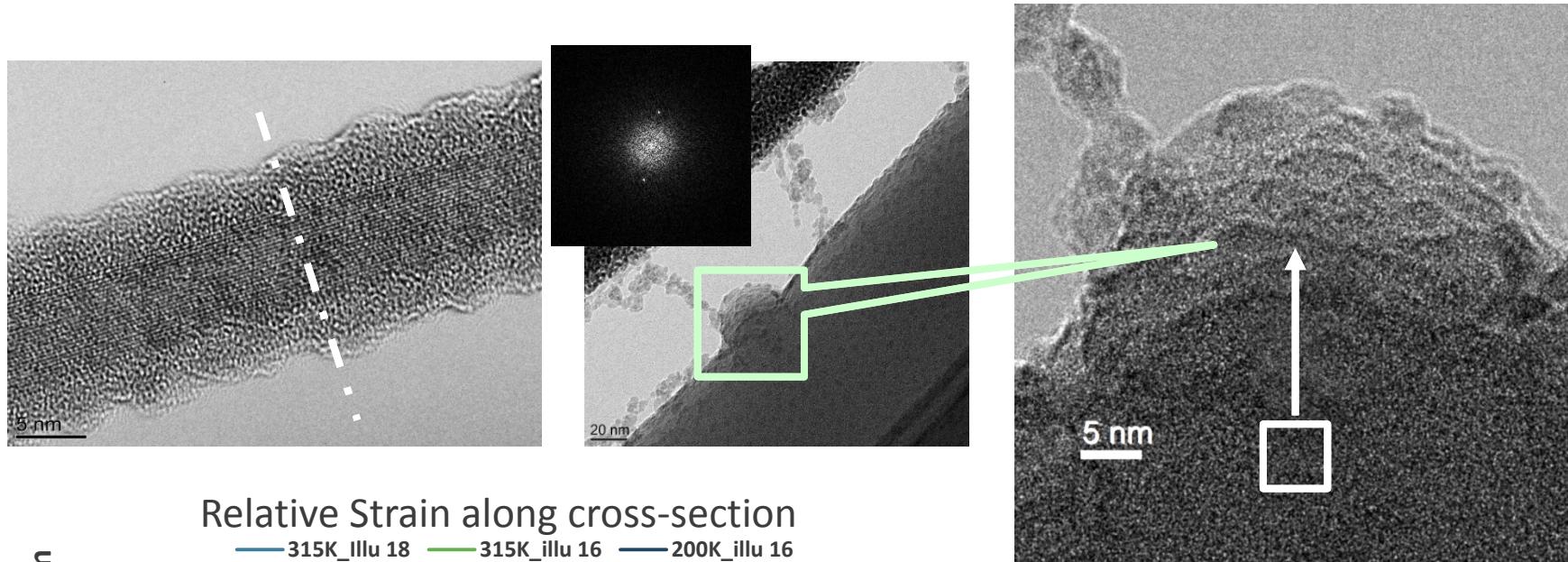
Population of low mass Γ valley

Y. M. Niquet Nano Lett 12, 3545 (2012)



A. Heinzig, et. al Nano Lett 13, 119 (2013)

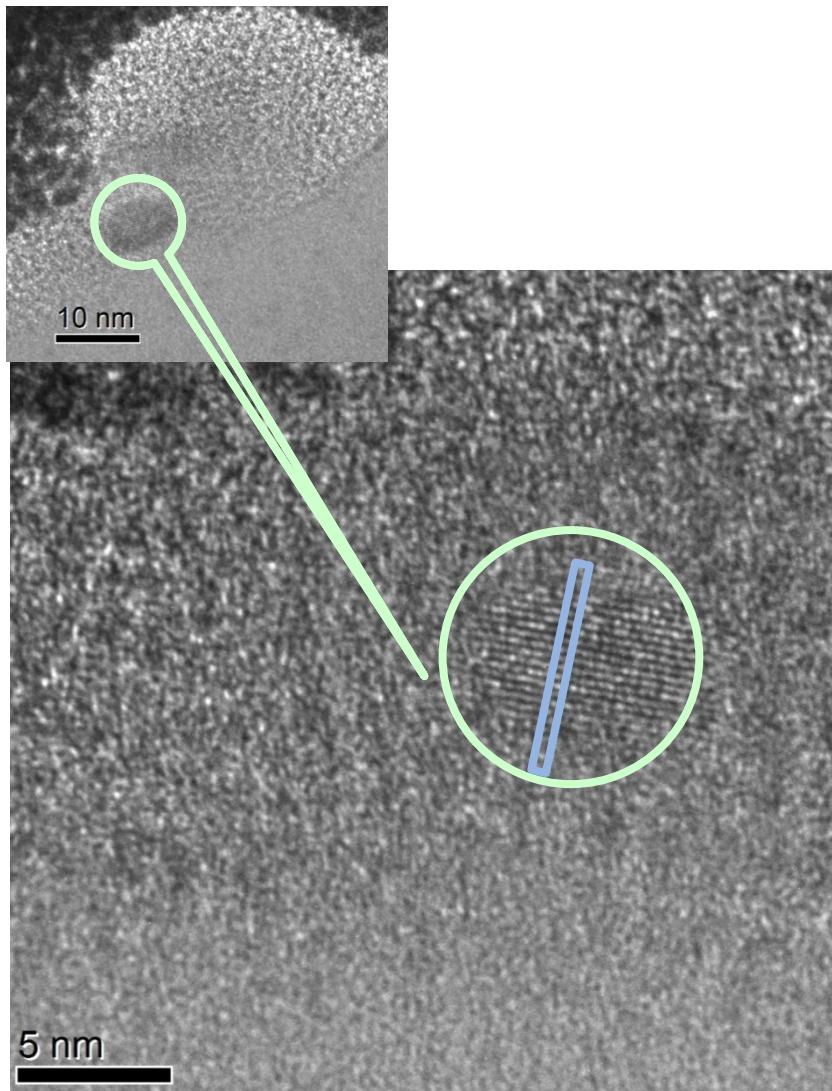
Strain mapping of <112> Si nanowire



Strain extracted from lattice spacing at different positions for different illuminations. Strain relaxation in the nanowire center. strongest compressive strain at nanowire surface



Cross-section analysis oxidized <110> Si nanowires



- Oxidation converts part of the nanowire to SiO_2
- Resulting crystalline nanowire diameter is reduced
- Typically, this leads to compressive strain
- Size has to be known for device modeling due to size effects

S. Banerjee, M. Löffler DCN
cfaed

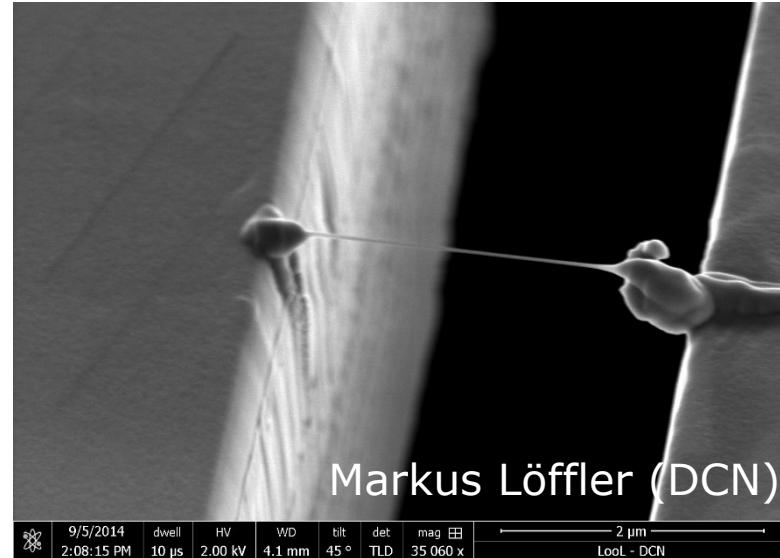
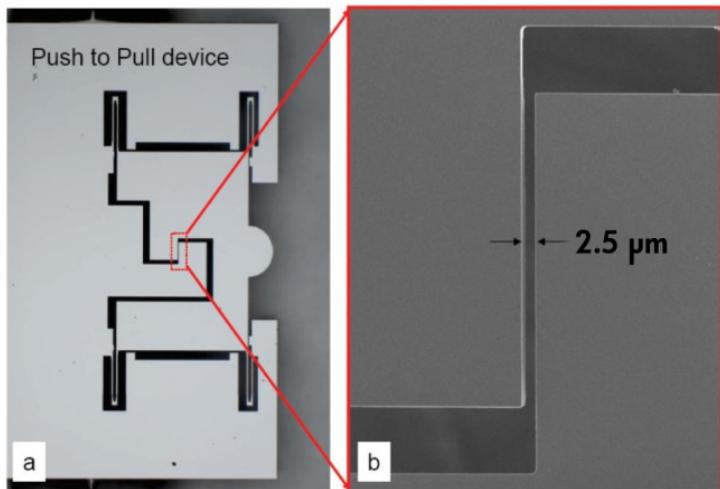
CENTER FOR
ADVANCING
ELECTRONICS
DRESDEN

dcn
dresden center for
nanoanalysis

Outlook: mechanical in-situ testing in the TEM



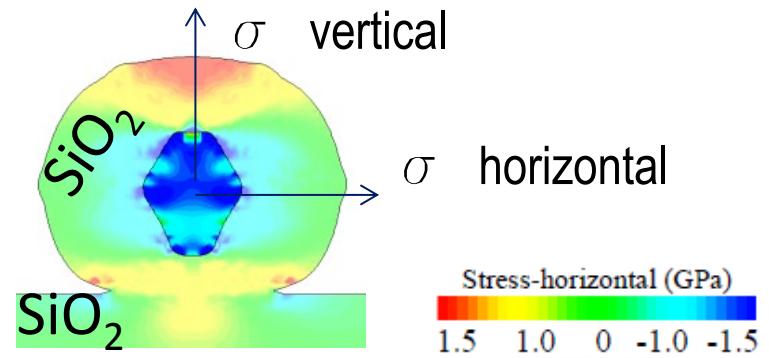
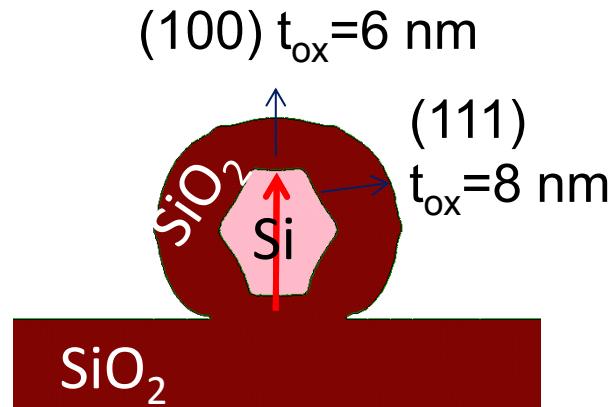
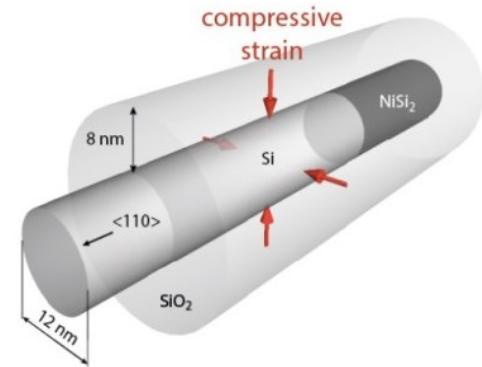
Using the Hysitron PI95 Indenter holder with push-to-pull MEMS chips



- Sample preparation with micromanipulation in the (FIB)SEM
- Measure strain-dependent bandgap and maximum tolerable strain

Radial compressive strain in Si nanowires

- Process simulation



- Same trend in strain distribution between HRTEM vs. process simulations
- Relaxation in nanowire center, highest compressive strain @ nanowire top surface
- Mean stress extracted from microRaman: -1.3 GPa (radial compressive)

Silicidation and Strain Analysis of Silicon Nanowires

Outline



Metal / silicon nanowire heterostructures



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Transistor applications

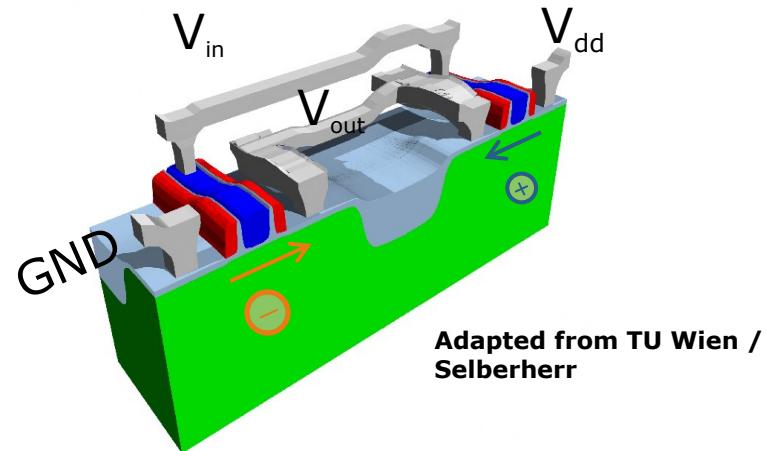


Summary

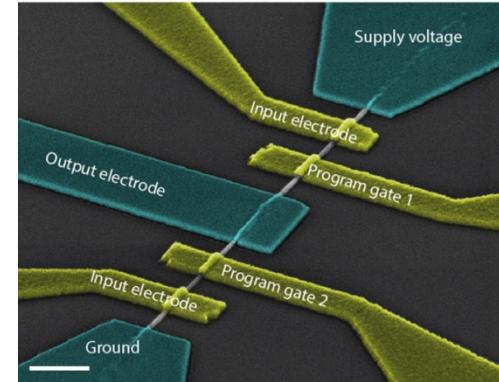
What we use silicide and strain for: Reconfigurable Transistors

Doping free silicon technology, giving unipolar p- and n-FET behavior from the same device as programmed electrically

Conventional CMOS inverter



Reconfigurable FET inverter

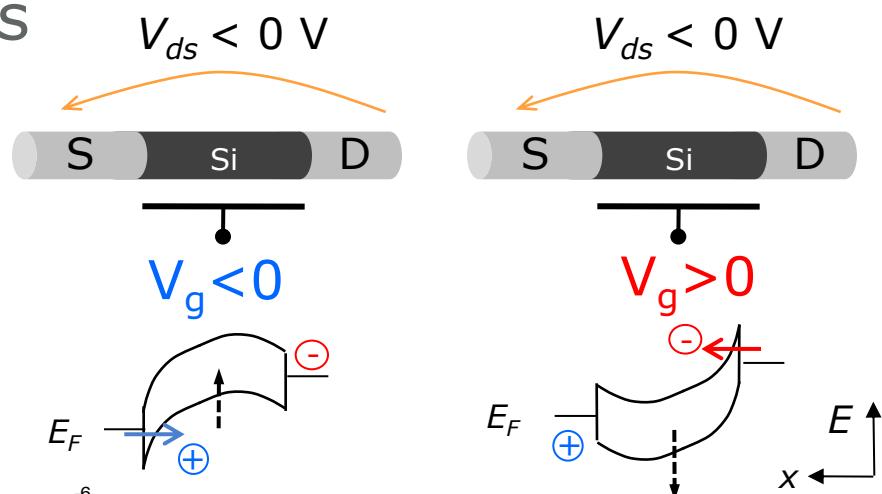


- Doping profiles needed
- Different width
- Different stressors for p- and n-FET
- STI needed to isolate p- n- FETs

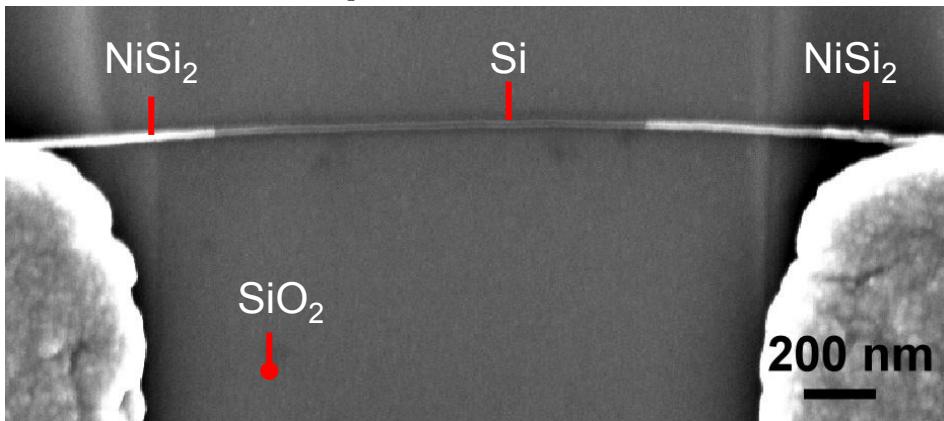
- No doping needed
- Single stressor
- Identical device for p- and n-FET
- No STI needed
- Two gates per device needed (self-aligned)

Working principle Schottky FETs

- Intrinsic-Si: depletion / accumulation
- Field induced band bending at junctions
- Injection of both electrons and holes
-> ambipolar behavior



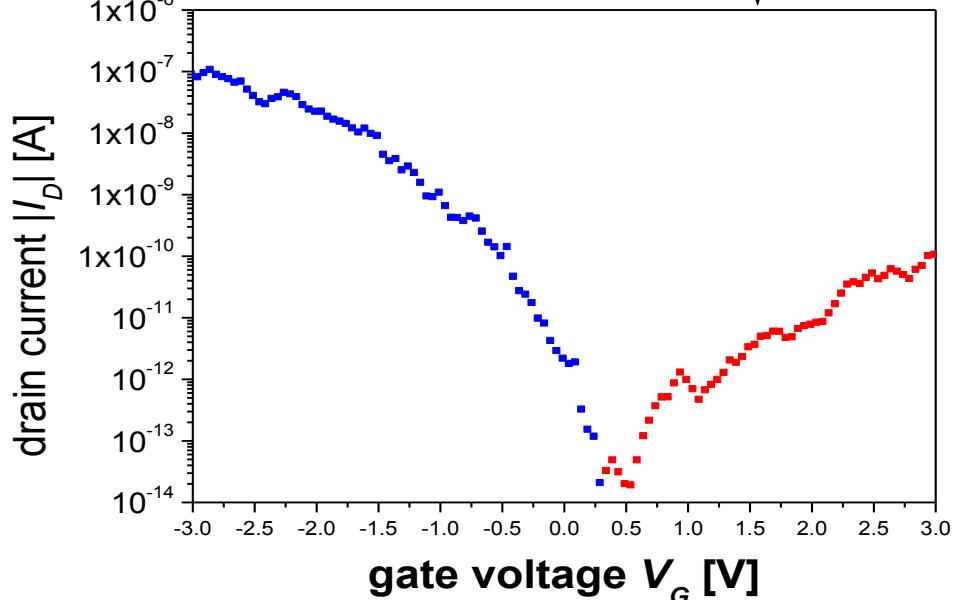
SEM top view of a Si-NW -FET



Reference: bulk NiSi_2/Si

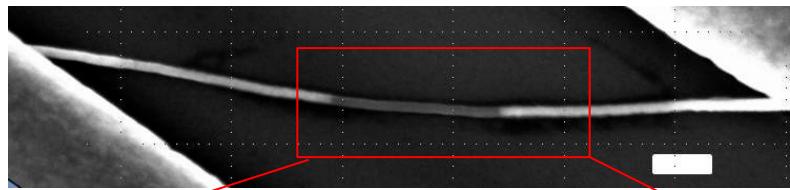
$$\begin{aligned}e\phi_B \text{ holes} &= 0.39 - 0.48 \text{ eV} \\e\phi_B \text{ electrons} &= 0.66 - 0.75 \text{ eV}\end{aligned}$$

-> How can we manipulate electron and hole injection?



Transport alteration in metal / Si / metal nanowires

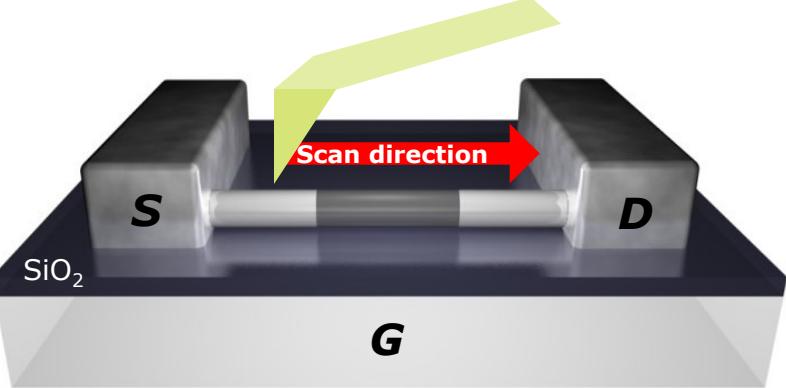
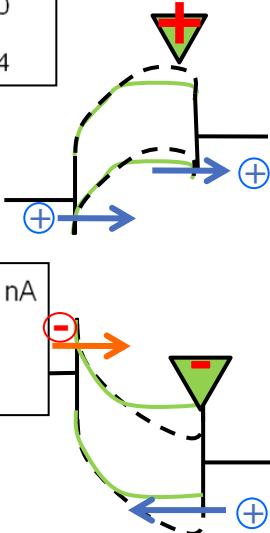
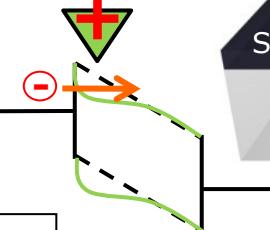
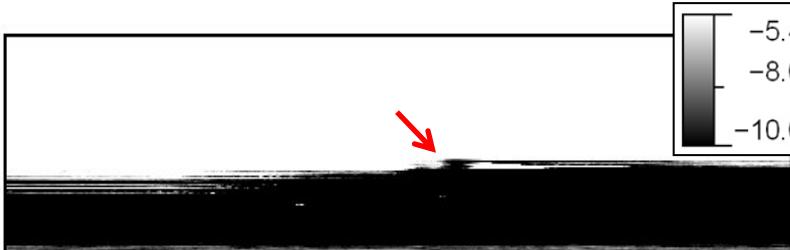
SEM



current - maps



drain



➤ Turn device on with electron tunnel current

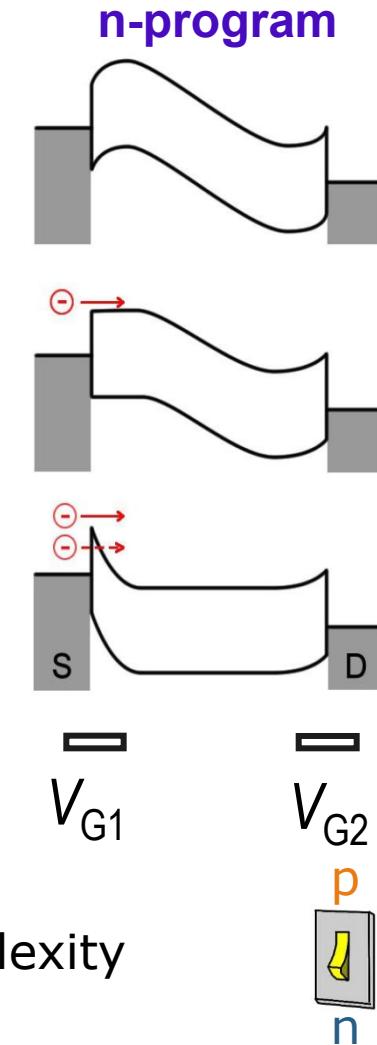
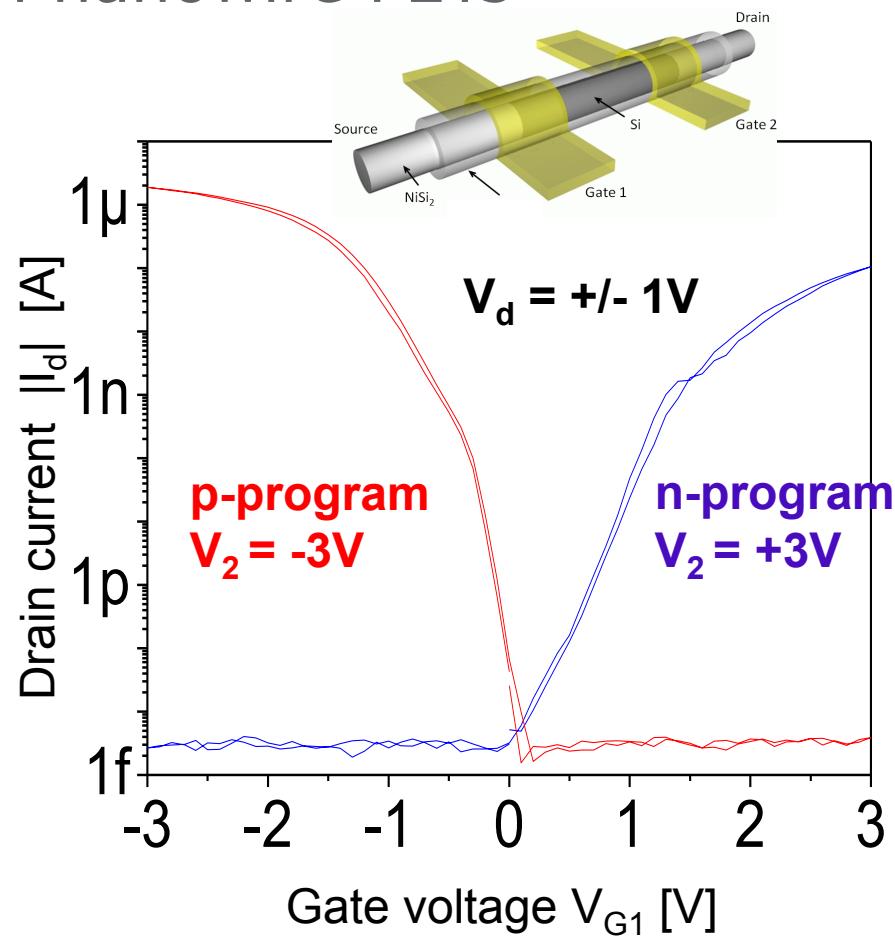
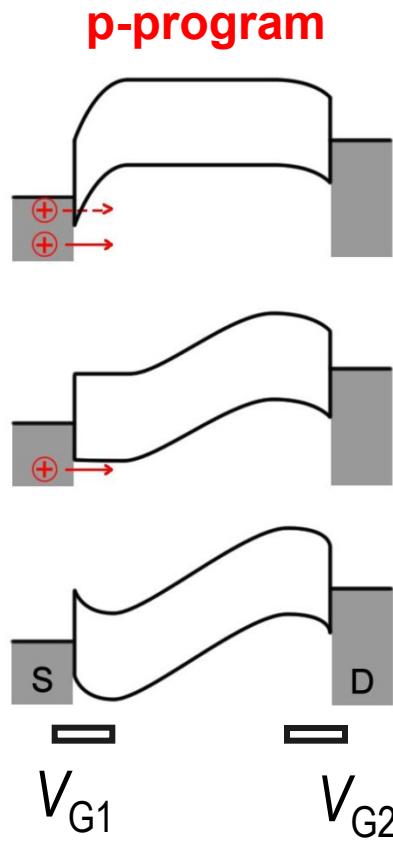
➤ Enhance on-current by flushing holes at drain

➤ Non-volatile program through charge trapping

➤ In contrast to a MOSFET a point potential selectively controls electron / hole transport

D. Martin, W. Weber et al. *Phys. Rev. Lett.* **107**, 216807 (2011)

Reconfigurable Si nanowire FETs



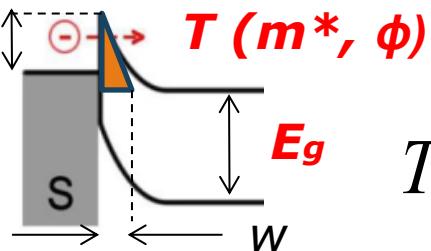
- Same FETs provide p- and n- type transport: leaner complexity
- Higher device functionality -> reprogrammable logic

$$I_{on} / I_{off} > 5 \times 10^7 ; J_{on} = 6 \times 10^5 \text{ A/cm}^2 @ Vd=1V ; g_m = 130 \mu\text{S}/\mu\text{m}$$

A. Heinzig, W. Weber et. al Nano Lett 12, 119 (2012)

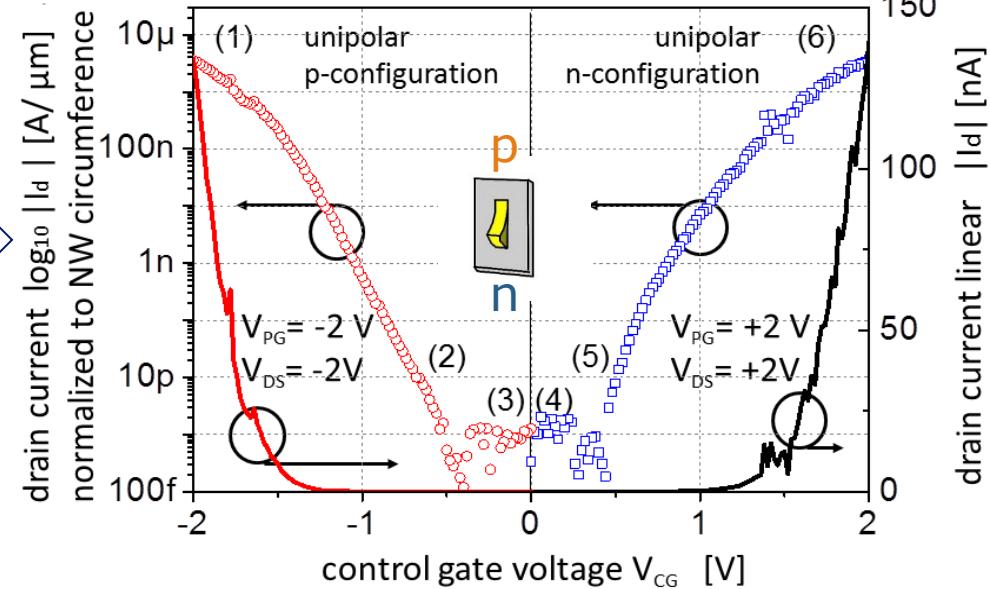
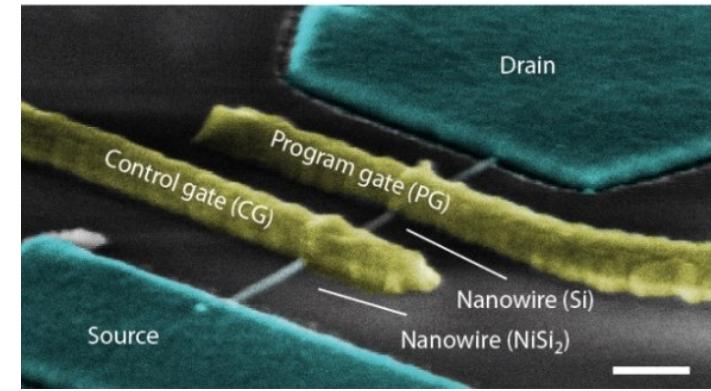
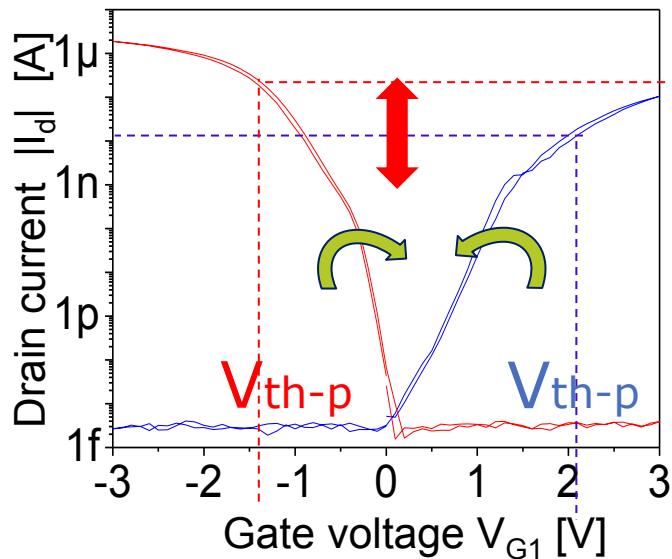
Strain to adjust tunneling currents

$e\phi n \rightarrow T(m^*, \phi)$



$$T \propto e^{-\frac{4w\sqrt{2m_{n,p}^*}\phi_{n,p}}{3q\hbar V}^{3/2}}$$

$$T \propto e$$



- V_{PG} filters undesired carriers in intrinsic channel; V_{CG} acts as regular gate
- Full symmetry, I_{on} , V_t by strain engineering

¹W. M. Weber et. al *IEEE Nanotech Proc.* (2008)

²A. Heinzig, et. al *Nano Lett* **12**, 119 (2012)

¹D. Martin et. al *Phys. Rev. Lett* **107**, 216807 (2011)

²A. Heinzig, et. al *Nano Lett* **13**, 4176 (2013)



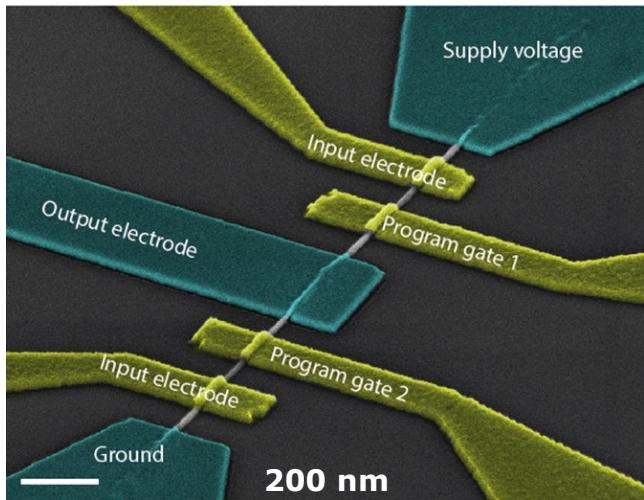
cfaed

CENTER FOR
ADVANCING
ELECTRONICS
DRESDEN

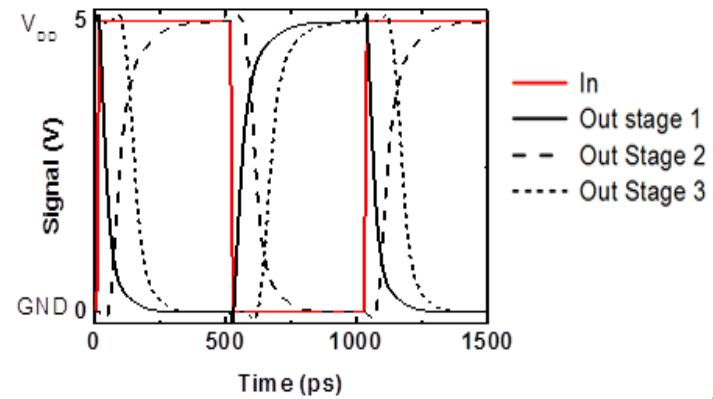
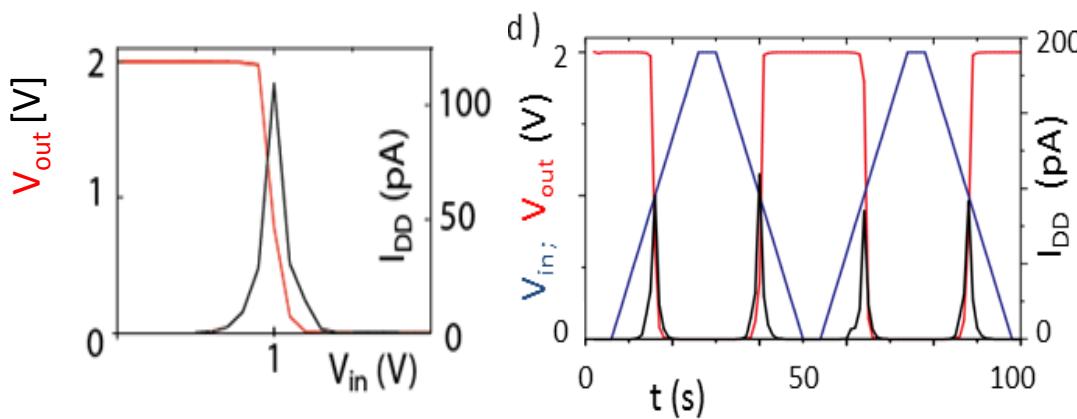
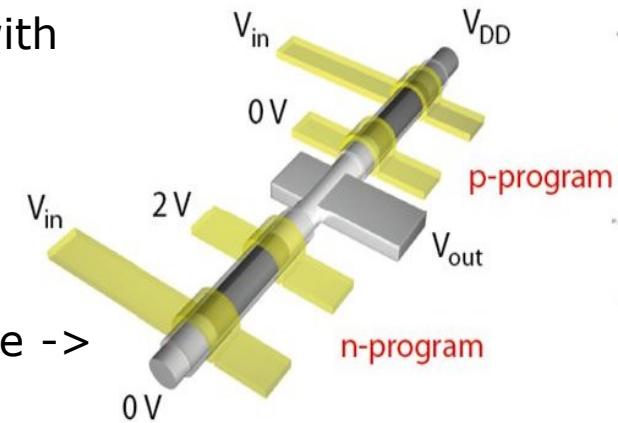


dresden center for
nanoanalysis

Complementary inverters integrated in 1-D



- Complementary operation with single V_{dd}
- Switching at $V_{dd} / 2$
- n/p fully exchangeable
- Capable of driving next stage -> Ultralow capacitances
 $C_L = 0.03 \text{ fF} \rightarrow 78 \text{ ps delay}$



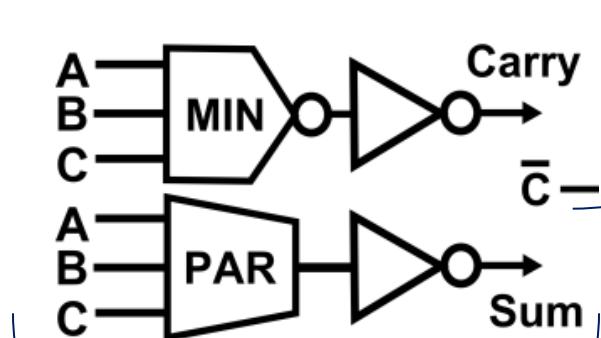
Mixed mode simul.

Benefit of reconfigurability at circuit level

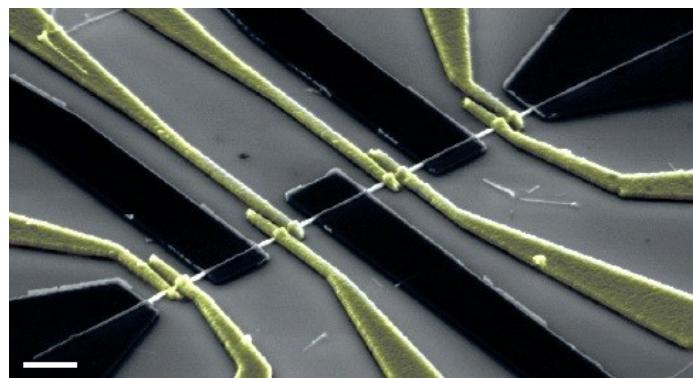
Reduction of transistor count and delay for main boolean functions

Example: 1bit full adder (needed for calculations and address decoders)

In CMOS 28 T needed



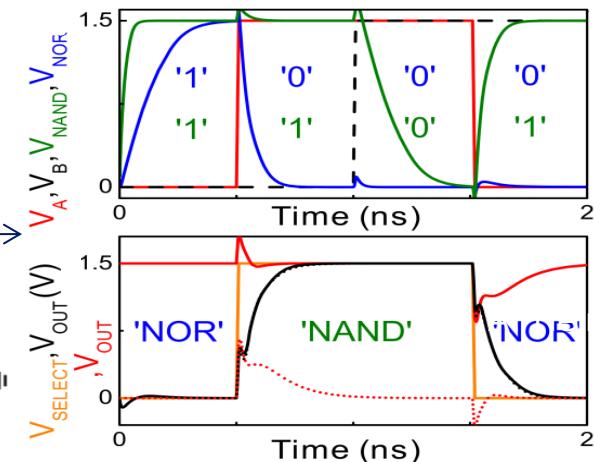
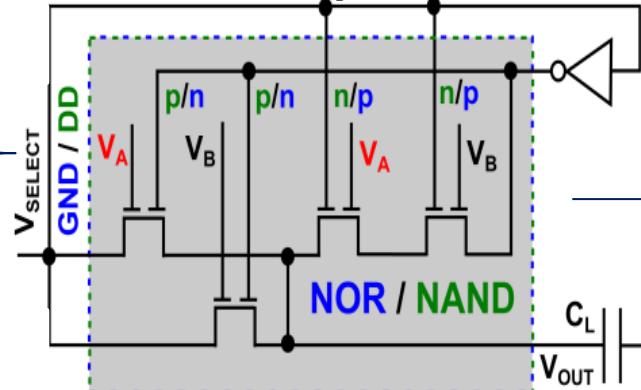
XOR/XNOR parity function



Basic 1 D cell

J. Trommer, A. Heinzig

6T NAND / NOR



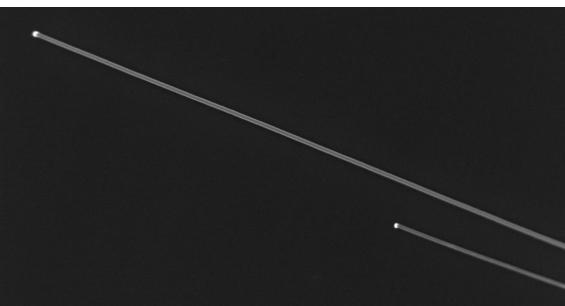
CMOS CARRY
RFET CARRY
CMOS SUM
RFET SUM
Structural Delay

-> 1-bit full adder with 14-T and up to 50% reduced structural delay

J.Trommer, et. al *Elec. Dev. Lett.* **35**, 141 (2014)

J. Trommer, et. Al. *ULIS-Euro - SOI* (2015)

Summary



Formation of metal / silicon nanowire heterostructures

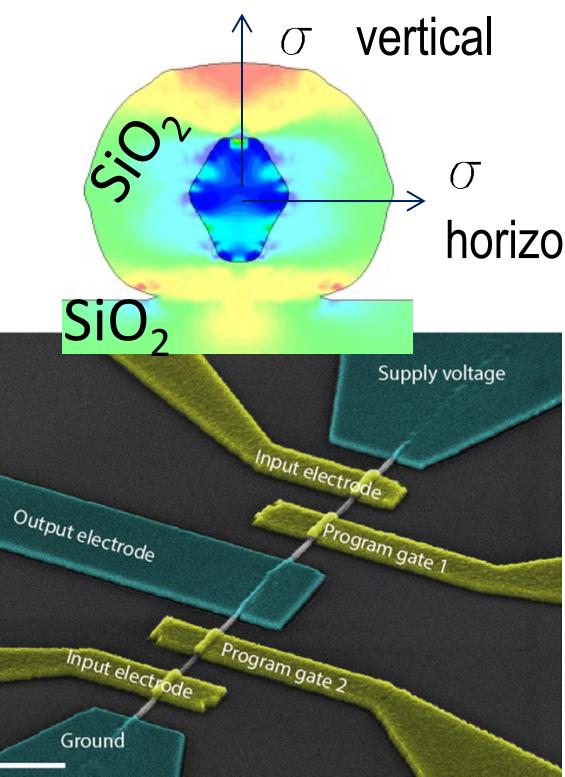
Reactions depend on size and crystal direction

Strain analysis in nanowires

Strain distribution is uneven along nanowire cross section and length

Transport properties

carrier type injected controlled by point potential



Reconfigurable electronics

p- and *n-* type behavior on the same devices

NAND \leftrightarrow NOR reconfigurable circuit string